AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:

a plurality of configuration memory cells;

at least one transceiver containing components having selectable values, said components being configured by said plurality of configuration memory cells, wherein one of said components is a loss of synchronization detector; and

wherein each transceiver has an input port that receives differential input signals and an output port that outputs differential output signals.

2. (Original) The integrated circuit of claim 1 wherein one of said components is a cyclic redundancy code generator.

3. (Original) The integrated circuit of claim 1 wherein one of said components is a cyclic redundancy code verification block.

4. (Original) The integrated circuit of claim 1 wherein one of said components is a serializer.

5. (Original) The integrated circuit of claim 1 wherein one of said components is a deserializer.

6. (Original) The integrated circuit of claim 5 wherein said deserializer further comprises configurable comma detection function.

7. (Original) The integrated circuit of claim 1 wherein one of said components is an elastic buffer.

Claim 8. (Cancelled)

9. (Original) The integrated circuit of claim 1 further comprising:

a programmable fabric; and

at least one signal generated by said programmable fabric for controlling said values of said components.

10. (Original) The integrated circuit of claim 9 wherein one of said components is an encoder, and said at least one signal controls said encoder.

11. (Currently Amended) An integrated circuit comprising:

a programmable fabric;

a processor core surrounded by said programmable fabric;

a plurality of configurable transceivers located at the peripheral of said programmable fabric, wherein at least one of said configurable transceivers comprises a loss of synchronization detector;

wherein each transceiver has an input port that receives differential input signals and an output port that outputs differential output signals; and

a plurality of signal paths connecting at least one of said configurable transceivers and said processor core, at least a portion of each of said signal paths passing through said programmable fabric.

12. (Original) The integrated circuit of claim 11 further comprising a plurality of configuration memory cells, and wherein some of said memory cells are associated with said configurable transceivers.

13. (Original) The integrated circuit of claim 12 wherein at least one of said configurable transceivers comprises a cyclic redundancy code generator and a cyclic redundancy code verification block.

14. (Original) The integrated circuit of claim 12 wherein at least one of said configurable transceivers comprises a serializer and a deserializer.

15. (Original) The integrated circuit of claim 14 wherein said deserializer further comprises configurable comma detection function.

16. (Original) The integrated circuit of claim 12 wherein at least one of said configureable transceivers comprises an elastic buffer.

Claim 17. (Cancelled)

18. (Original) The integrated circuit of claim 11 wherein said programmable fabric generates at least one signal for controlling at least one of said configurable transceivers.

19. (Original) The integrated circuit of claim 18 wherein at least one of said configurable transceivers comprises an encoder, and said at least one signal controls said encoder.

20. (Currently Amended) An integrated circuit, comprising:

programmable fabric circuitry, including a plurality of configuration memory cells that are programmable to implement a circuit in the programmable fabric circuitry;

a processor core disposed on the integrated circuit, wherein the programmable fabric circuitry is configurable to couple to the processor core;

a plurality of configurable transceivers located at the periphery of the programmable fabric, each configurable transceiver including a configurable serializer and a configurable deserializer coupled to at least one of the configuration memory cells, wherein each serializer is configurable to transmit data at a selected ~~one of at least two~~ bit rate[[s]], and each deserializer is configurable to receive data at a selected ~~one of at least two~~ bit rate[[s]]; and

a plurality of signal paths coupling at least one of said configurable transceivers to the processor core, at least a portion of each of said signal paths passing through said programmable fabric circuitry.

21. (Previously Presented) The integrated circuit of claim 20, wherein each deserializer detects commas in received data and is configurable to detect one of at least two different definitions of a comma.

22. (Previously Presented) The integrated circuit of Claim 20, wherein at least one of said configurable transceivers comprises a loss of synchronization detector.